REALIZING THE PROMISE OF SILICON PHOTONICS

JOHN FERGUSON
MENTOR, A SIEMENS BUSINESS

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The goal of photonics is to use light to perform functions traditionally handled by electronics, such as communications, data transmission, information processing, etc. Photonics as a practical endeavor began with the invention of the laser in 1960. While inventions such as fiber-optics for transmitting information helped spur the broad adoption of photonics technology in the telecommunications industry, photonics are now used in a wide range of technology applications, including medical diagnostics, biological and chemical detection, manufacturing, etc. However, the cost of manufacturing photonics devices has limited their commercial availability.

Silicon foundries have been successful manufacturing silicon wafers in large volumes for years. These large volumes bring down costs, making silicon-based electrical integrated circuits (ICs) both affordable and profitable. At the same time, the development of design rule decks and process development kits (PDKs) helped standardize and optimize the design and verification of ICs across the industry, making it practicable and profitable for design companies to create the vast collection of ICs and intellectual property (IP) that exists in the market today.

As it turns out, silicon surrounded by silicon-oxide makes an almost ideal waveguide material, meaning optical signals can travel through it with very little degradation, a critical factor in creating marketable silicon photonics designs. While we certainly have had successes over the past decade, why haven't silicon photonics ICs (PICs) been more readily adopted on a larger scale? With all their advantages (transmission speed, low power usage, older proven processes, etc.), combined with the cost efficiencies of silicon wafer production, why haven't they taken over the market yet?

The basic answer: the scaling enabled through silicon foundries is built on and tailored to transistor-based technologies. One part of this is simply inertia. Foundries have a lot of experience and success tied into the Moore's Law model of ICs. While a 7 nm process today is very different from, say, a half-micron process 20-30 years ago, the improvements and advancements were achieved incrementally over time with each new node. It was always easier and cheaper to slightly modify existing mechanisms and processes than to start from scratch with something completely new.

However, Moore's law is now limping along. Yes, we can safely say there will be a 3 nm node, but it won't bring the performance or area benefits that previous node shrinks accomplished, and it will for sure come with a hefty price tag. This implies an opportunity for an inflection in the market. But what will PICs need (other than the opportunity) to be successful on anything resembling the scale ICs have achieved?

One answer lie in the standardization and optimization achieved by ICs. We need to replicate the machine that is the fabless infrastructure to work for a photonics-based world. This is easier said than done, of course. But we can begin by taking a closer look at that infrastructure and its history to understand the effort required.

Let's consider what a fabless IC team receives from their foundry when designing a system-on-chip (SOC). First, there is the PDK. The PDK essentially represents an implied contract that the appropriate electronic design automation (EDA) software tools, if used appropriately, will work to enable a manufacturable, operable design in the target process. At the heart of the PDK are the design rules, which define the manufacturing requirements for physical layouts. Design rule checking (DRC) ensures that the geometries created in a layout can be successfully manufactured in the given foundry process. To support the design rules, the foundries must also declare which layers on an incoming GDS or OASIS file are used for which process steps used to create the appropriate masks.

The next part of the PDK is the device models. Foundries are experts at transistor science. They meticulously characterize exactly how a transistor will perform in a given construct. As long as the designers build the transistors correctly, they can have confidence that the devices will perform as designed.

However, device models alone are insufficient for scaling. If designers had to focus on making sure every single transistor in the layout was assembled correctly, it would take eons to design the multi-billion transistor SoCs that we create today.

To enable this scaling, the PDKs add more information. First are pre-characterized cells (Pcells). Pcells allow the designer to select among a set of known and allowed parameters that can be modified within a range to enable different electrical behaviors for a transistor or a set of transistors. More importantly, these parameters can be driven through a pre-determined and characterized design in the form of a circuit schematic. This schematic-driven design approach allows the designer to focus on design intent rather than physical layout, greatly improving throughput. To further simplify the process, the PDK provides schematic symbols with allowed parameters, which designers can use to ensure their intended design can be achieved with the building blocks provided.

Of course, even that is not enough. To go further, the foundries also provide pre-characterized standard cell libraries. These libraries represent commonly used logical gates and other relatively simple building blocks. The foundries also provide larger IP blocks and/or characterize and approve IP from 3rd-party providers for components like memories, processors, etc. Theoretically, SoC designers can combine any or all of these to their liking, and be confident in their behavior and performance.

But even that is not so easy. How do we know how well these pieces will perform together? This is where the digital design flow truly blossoms. Standard cells and IP come with timing libraries to give designers an idea of how they will behave when combined together in a layout. Rather than detailed analysis, these timing libraries provide corners, which indicate the component's behaviors under certain conditions. With the addition of some parameters, typically in the form of LEF libraries and tech files, these libraries can be used to direct a design flow that can both validate timing and also drive layout through place and route (P&R) tools.

Yet even with all of this, an IC design flow is far from push-button, and it is still very possible and relatively easy to make a mistake that results in yield or reliability problems. Still, given their overall history of success, you can see why designers are reluctant to abandon all of this infrastructure and security.

What does that mean for silicon photonics? It means that the development of similar tools and components are essential to integrating PICs into the traditional IC design and verification processes, starting with the development of a photonics PDK.

Actually, despite the challenges, there has been good progress towards achieving this goal. Despite the fact that the GDS and OASIS file formats do not natively support the curved structures common in PICs, and that traditional DRC verification of these structures results in thousands of false errors, we have successfully enabled methods that allow a dedicated DRC run to check PIC layouts for real layout problems without flagging false errors.

We are not yet at a point of having true pre-characterized photonics devices complete with a Pcell definition, but we are close. The ability to create such Pcells can be achieved through the use of Python™-based Pcells (Pycells), or by using tools like the PhoeniX OptoDesigner design platform or Luceda IPKISS.eda design framework [1][2][3]. Calibre® nmLVS™ circuit verification

can perform simple device black box style layout vs. schematic (LVS) verification to ensure no shorts or opens exist in the generated layout, and pass the rendered optical design as extracted from the layout to optical simulators such as Lumerical's Interconnect circuit design tool [4][5]. Mentor recently released enhancements to the Tanner L-Edit tool that enable manual layout of integrated photonic designs. In the near future, Mentor will offer the industry's first integrated electrical/photonic layout automation tool. The resulting designs will be "correct by Calibre" and fit into an OpenAccess design flow. Together these tools and processes represent a significant advancement that can help lead photonics designers away from focusing on device component differentiation toward designing based on known and pre-characterized structures.

The EDA industry realizes there are still big hurdles to get over. Our foundry partners are transistor experts, but they are far from optical experts. We can help. With an appropriate process model, which can be generated based on post-silicon measurements, we can predict how the drawn PIC layout will render through the manufacturing steps. We can automatically capture the differences between the intended layout shapes and the final form of the manufactured shapes. In this way, we can enable a foundry or a design team to characterize a device by generating layouts across multiple versions of possible physical parameters to determine how the differences will impact optical behavior. From this characterization, a better understanding of allowable combinations of allowable parameters will eventually enable the generation of certified/qualified Pcells for PICs.

Unlike the transistor, for which the electrical behavior is largely characterized by width and space, it is far more difficult to verify the intended electrical behavior of an optical device based on its layout, or even silicon image, without doing full simulation. Fortunately, that may not be necessary. The idea behind LVS device verification is to assure that the layout adequately represents the intent. An alternative approach is simply to re-render the intentional shape to the placement in context. If no changes are found, then designers know the placed device matches the intended device. There are several approaches that can be used for this comparison, from complex pattern matching to simply regenerating based on the optical equations.

But there is still one last issue to consider—how to successfully combine photonics and electronics components. In the ideal case, designers would put the required electrical and photonics components together on the same die. But, photonics components are generally quite large, compared to their electrical cousins, and they do not need or use advanced node processes. If designers need electronics capabilities that are only enabled by advanced nodes to drive the photonics components, they would end up using lots of very expensive area for the photonics components, making the final SOC price-prohibitive. In fact, given the large size of photonics components, trying to combine them with electronic components on one chip may also drive the die size up, increasing the costs even more.

The obvious solution here is multi-die packaging, and the news in that regard is quite good. A great deal of progress has been achieved with foundries and outsourced assembly and test (OSAT) companies alike in the development of PDK-like approaches to simplify and reduce the risks of package design and verification. In fact, TowerJazz, a leading-edge foundry in silicon photonics production, recently released its initial silicon photonics PDK based on the industry-leading Calibre nmPlatform. With Calibre nmPlatform support, customers targeting TowerJazz's PH18 silicon photonics process now have the same high level of confidence that they are constructing physically-correct silicon photonics devices as they have always had for complementary metal-oxide-semiconductor (CMOS) devices [6].

Silicon photonics offers up the promise of blazing fast data transmission and high bandwidth, with low power consumption—essential for today's high-performance computing, telecommunications, military, defense, aerospace, medical, and research applications. However, to realize that promise, design companies must have the same level of support provided by foundries and EDA suppliers for the design and verification of ICs. Fortunately, the prognosis is good! The industry is actively engaging between foundries, designers, EDA suppliers, and OSATS, with commitments to continue and expand on the progress achieved thus far, with the ultimate goal of attaining the inexpensive and scalable platform needed to move silicon photonics to a true production design offering.

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Corporate Headquarters
Mentor Graphics Corporation
8005 SW Boeckman Road
Wilsonville, OR 97070-7777
Phone: 503.685.7000
Fax: 503.685.1204

Sales and Product Information
Phone: 800.547.3000
sales_info@mentor.com

Silicon Valley
Mentor Graphics Corporation
46871 Bayside Parkway
Fremont, CA 94538 USA
Phone: 510.354.7400
Fax: 510.354.7467

North American Support Center
Phone: 800.547.4303

Europe
Mentor Graphics
Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics (Taiwan)
11F, No. 120, Section 2,
Gongdao 5th Road
HsinChu City 300,
Taiwan, ROC
Phone: 886.3.513.1000
Fax: 886.3.573.4734

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Trust Tower
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140-0001
Japan
Phone: +81.3.5488.3033
Fax: +81.3.5488.3004

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