RETHINKING APPLICATIONS PROCESSING FOR ULTRA-LOW POWER – i.MX 7ULP

INTRODUCTION

The world is full of tradeoffs. You can't have Falstaff and have him thin; you can't eat your cake and have it, too; and there's no such thing as a free lunch. Every designer knows that you can't increase a processor's speed without increasing its power consumption. Slow the clock to save power and performance sinks. Compensate by doing more work per cycle and power rises back up. Jettison functions and power goes down — and with it the chip's usefulness. Similarly, ease of use dwindles if developers must rely solely on bare-metal code executing on an MCU-class core to eke out performance with less overhead instead of having the option to write rich applications running on a high-level OS. Ultimately, compromise is inevitable in a world of tradeoffs governed by the laws of physics — unless you're clever and rethink the application processor. This is exactly what NXP has done with the i.MX 7ULP applications processor.

Sometimes the name says it all. NXP built the i.MX 7ULP applications processor with a singular focus on ultra-low power — in all modes, regardless of whether the processor is running or standing by.

To achieve this goal, NXP chose clever techniques to dramatically reduce power without severely compromising features and performance. The result is a device that can run Linux® or another high-level OS and that includes application-processing functions like a GPU, USB connectivity, and NXP's renowned platform security to help enable secure boot and implement simple tamper detection. Consuming as little as 50µW while in deep sleep and 200mW with its application CPU running at full speed, the i.MX 7ULP helps enable systems to be powered by coin-cell batteries. Here's how the i.MX 7ULP processor does it.

At the most fundamental level — transistor structure — NXP reduced the i.MX 7ULP power by fabricating it in a 28nm fully-depleted silicon-on-insulator (FD SOI) process. An SOI process builds a CMOS transistor on top of an oxide layer buried in the silicon wafer. This reduces the parasitic capacitances in the transistors, such as between the source and drain and the wafer substrate, reducing the power lost to charging these capacitors every time the transistor switches. The buried oxide also inhibits current from leaking from transistors

to the substrate, again saving power. Leakage is further controlled by adjusting the bias voltage of the substrate, which can be done dynamically in FD SOI circuits. The bias affects leakage by changing transistors' threshold voltage (Vt). Raise Vt to increase switching speed; lower it to save power. Moreover, lower device voltage (Vdd) is needed to achieve the same transistor speed with FD SOI, reducing dynamic power consumption. The FD SOI process is essential to minimizing the i.MX 7ULP power consumption in all modes, shifting the frame of reference from integer watts typical of application processors to milliwatts and microwatts.

CAPABILITY WITHOUT COMPROMISE

NXP carefully chose the function blocks included in the i.MX 7ULP processor to minimize power without compromising device capability. As with other i.MX 7 devices, the i.MX 7ULP has an Arm® Cortex-A7 CPU at its heart. With an MMU, Level 2 cache, FPU, Neon vector unit, TrustZone security mode, and embedded trace module, the Cortex-A7 core is a fully-featured 32-bit CPU ideal for hosting a high-level operating system. Compared with the older Cortex-A9 CPU used in the i.MX 6 series, the Cortex-A7 CPU delivers slightly less instruction throughput at a given clock rate. However, it consumes far less power. Its power efficiency is, therefore, about 1.6x that of the Cortex-A9 CPU.

NXP also integrates a 3D GPU in the i.MX 7ULP chip without compromising power consumption. In fact, it's the only i.MX 7 family member with a 3D GPU. Like other GPUs in the i.MX portfolio, this GPU comes from Vivante. This single-shader GC7000 Nano Ultra GPU is fully-featured, supporting OpenGL and OpenVG but scaled down to conserve power. It's plenty powerful for a small screen, such as on a wearable. A GPU for a high-resolution cell phone or TV screen would provide no benefit in such an application and unnecessarily consume power.

Complementing the GPU is a GC320 composition engine. Supporting popular 2D APIs and numerous 2D functions, such as transformations, drawing functions, and color conversion, its role is to blend graphic elements like a background, user interface elements, and 3D graphics. This engine provides another option to save power: developers can turn off the 3D GPU and rely solely on the 2D composition engine. Doing this may reduce power by 90%.

Underscoring the commitment to capability without compromise, the i.MX 7ULP integrates an Arm® Cortex-M MCU-class CPU core like other members of the i.MX 7 and i.MX 8 families. In the i.MX 7ULP applications processor, this is a Cortex-M4 core with a small cache and 256 KB of tightly-coupled memory. This core has an FPU and DSP extensions, enabling it to perform not only real-time control functions but also signal processing. This CPU anchors the real-time domain in the i.MX7 ULP device, as shown in Figure 1, below. This domain has timers, debug facilities, platform security functions, connectivity, a QSPI port to memory, and 12-bit ADCs and DACs. It's as though NXP fused a microprocessor and an MCU. Simply combining these two elements in one chip reduces system cost and power consumption compared with the two-chip alternative.

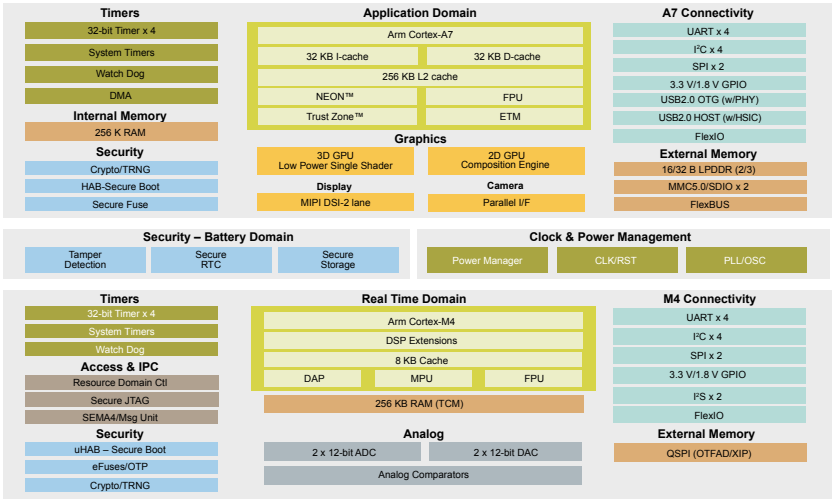

Figure 1: Block Diagram of NXP i.MX 7ULP Applications Processor

The big power savings, however, comes from how NXP fused MPU and MCU domains. Blocks within an SoC typically share power, clocks, and buses. In the i.MX 7ULP processor, the application domain based on the Cortex-A7 core and the real-time domain based on the Cortex-M4 core have separate power, clocks, and buses. This enables a design to suspend one domain while keeping the other active, maximizing power savings. A developer can use the lower power real-time domain continuously for background tasks and activate the application domain only when the system must interact with a person, for example. NXP calls this approach heterogeneous domain computing. It builds on the idea of heterogeneous computing, which focuses on improving performance or responsiveness by employing dissimilar processing resources, and by using these resources selectively to save power.

THE I.MX 7ULP APPLICATIONS PROCESSOR IN ACTION

The power thriftiness of the i.MX 7ULP applications processor brings the benefits of a rich OS to battery-powered devices. For these devices, battery capacity limits their design. Wearables, for example, require physically small batteries to be comfortable but can be recharged daily. Other devices, such as certain home and industrial automation systems, may need to run for months on battery and have fewer constraints on battery size. A key design parameter, therefore, isn't power but rather energy — energy multiplied by time. For these designs, what matters isn't how little power a processor uses in a single mode but how little it uses in all modes, minimizing energy consumption and maximizing battery life.

Smartwatches are popular wearables and contain batteries that hold only 300 mAh of energy. At the same time, they must deliver a smartphone-like user experience. Fortunately, it must only deliver this experience while the user is looking at it. This is a perfect fit for the i.MX 7ULP processor. The GPU or 2D compositing engine renders the user interface (UI) when the watch wearer raises his wrist and can otherwise sleep. With the UI active, the Cortex-A7 domain awakens and runs the required applications.

The rest of the time, the Cortex-M4 domain is in charge, working as a real-time sensor hub, gathering accelerometer data to count steps or detect the user turning the watch to gaze at it, exchanging data via Bluetooth with the user's smartphone, logging GPS data, and capturing temperature readings. This domain has the analog and digital interfaces required to communicate to these off-chip sensors. Meanwhile, the application domain is sound asleep consuming minimal power yet remains able to wake up nearly instantaneously. Figure 2 below is a block diagram of a typical smartwatch.

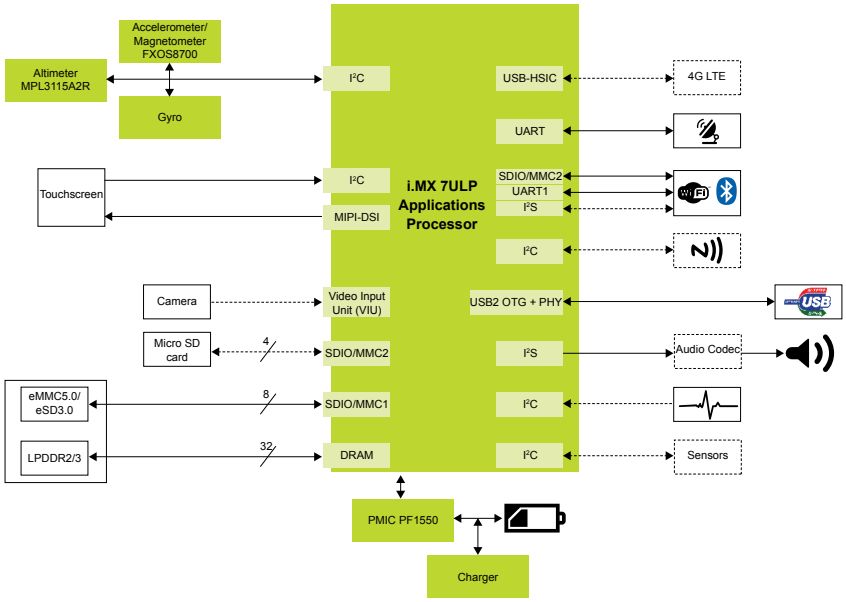

Figure 2: Smartwatch Based on the NXP i.MX 7 ULP Applications Processor

Smart locks differ. They can house four alkaline AA batteries instead of coin cells or custom lithium-ion power packs. Unlike a wearable that's charged daily, a homeowner changes these batteries only annually. The lock also might have no screen but have a camera to record who comes to the door. This image unlocks the door if artificial intelligence (AI) algorithms running on the smart lock recognize the person. Easing the development task, the application domain of the i.MX7 ULP processor includes camera interfaces, and the Cortex-A7 CPU with Neon extensions is powerful enough to run AI algorithms suitable this kind of home automation.

Figure 3: Smart Lock

A smart lock is quiescent an even greater percentage of time than a smart watch. A system design might not have the application domain sleep but cold boot it when its services are required. A highly-optimized Linux image can boot fast from flash. Alternatively, the application domain can hibernate, storing state in off-chip LPDDR memory and putting this memory in self-refresh mode. The ever-vigilant real-time domain handles control functions like triggering the sliding bolt and monitoring key presses and proximity sensors. For even more aggressive power saving, the i.MX7 ULP applications processor can power-off everything but its real-time clock.

The i.MX 7ULP processor is also well suited to devices tracking conditions in remote facilities, shipping containers, and warehouses. The processor connects to temperature and humidity sensors to monitor environmental conditions, an accelerometer to record tipping or dropping, and GPS to track location, such as in the following scenario. Powered by a 4000 mAh or bigger battery, a monitoring device runs unattended for a year, perhaps attached to a pallet or shipping container. Periodically the real-time domain wakes up and gathers sensor data. If it wakes up at a warehouse, it wakes up the application domain running communications software. This software logs onto the warehouse's network and uploads the sensor data collected by the real-time domain. The warehouse will, therefore, learn how shipped items were handled during transport.

To aid development of such devices, NXP offers the i.MX 7ULP Evaluation Kit (EVK) shown in Figure 3. A system-on-module (SOM) board, the EVK has 1GB of LPDDR3 memory, 8MB of quad-SPI flash, a Micro SD socket, Wi-Fi/Bluetooth capability, USB connectors, and an NXP PF1550 power management IC. The SOM plugs into a baseboard with a full SD/MMC card socket, audio codec, sensors, an HDMI connector, and an MIPI display connector. It supports Linux®, Android™, and FreeRTOS. More information is available at https://www.nxp.com/IMX7ULPEVK.

Figure 4: NXP's i.MX 7ULP EVK

CONCLUSION

Having rethought the application processor, NXP enables developers to do the heretofore unthinkable: create systems with graphical user interfaces, cameras, AI, and networking capability based on a rich operating system that runs on battery power for hours, days, or longer. In a world of seemingly impossible-to-avoid tradeoffs, the i.MX7 ULP applications processor stands out for requiring developers to make so few. The device and EVK are available now. Running the Cortex-A7 CPU at 720MHz, the i.MX7 ULP can keep power below 200mW. In deep sleep mode, power consumption can reach as low as 50µW for efficient configurations. With the Cortex-M4 using lower voltages in the Very Low Power Run Mode, core power can achieve efficiency levels of 35µW/MHz. For more information, see https://www.nxp.com/imx7ulp.

HOW TO REACH US

Home Page: www.nxp.com
Web Support: www.nxp.com/support

USA/Europe or Locations Not Listed:
NXP Semiconductors USA, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or +1-480-768-2130
www.nxp.com/support

Europe, Middle East, and Africa:
NXP Semiconductors Germany GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.nxp.com/support

Japan:
NXP Japan Ltd.
Yebisu Garden Place Tower 24F,
4-20-3, Ebisu, Shibuya-ku,
Tokyo 150-6024, Japan
0120 950 032 (Domestic Toll Free)
www.nxp.com/jp/support/

Asia/Pacific:
NXP Semiconductors Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@nxp.com

JOE BYRNE

MARKETING MANAGER

Joseph Byrne is part of the marketing team in NXP's edge processing group. He has served NXP and Freescale in various marketing roles, marketing NXP's processors to networking customers, managing a strategic marketing group, and managing software for Layerscape processors. Having started his career in the semiconductor industry designing CPUs, Mr. Byrne went on to have a career in industry analysis and consulting before joining the team at NXP. He has a degree in engineering from Duke University and an MBA from the University of Michigan.

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